OIPE
DEC 2 8 2004
JC25
PATENT & TRADEMARK OFFICE

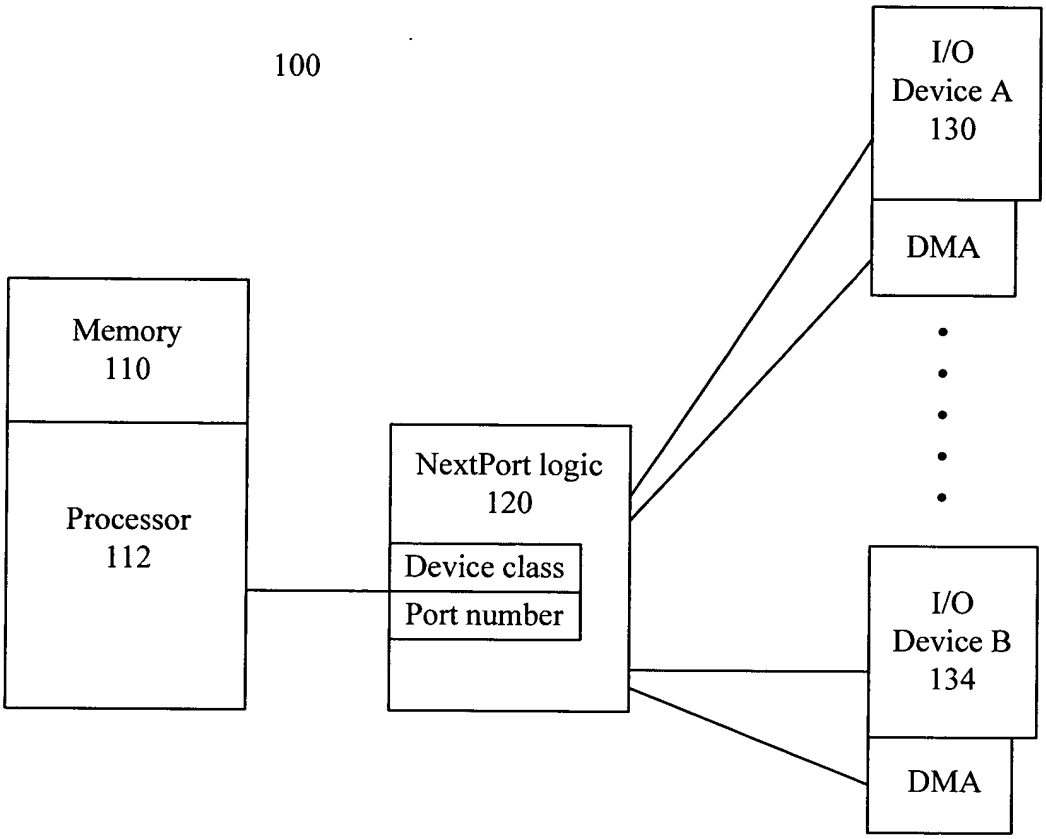


Figure 1

Table entry for Device A	Context pointer	Handler routine address
Table entry for Device A DMA	Context pointer	Handler routine address
Table entry for Device B	Context pointer	Handler routine address
Table entry for Device B DMA	Context pointer	Handler routine address
•	•	•
•	•	•
•	•	•

Figure 2

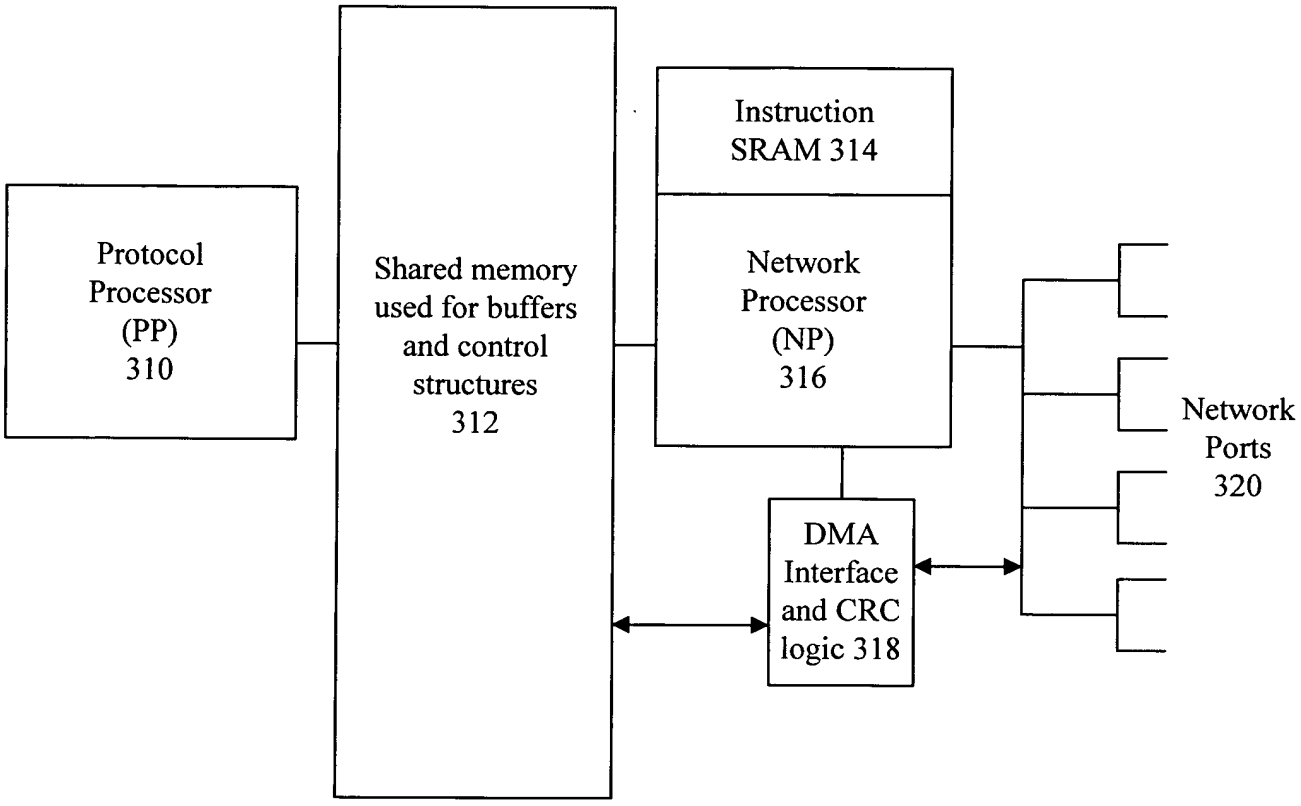

Protocol Processor (PP) 310
Shared memory used for buffers and control structures 312
Instruction SRAM 314
Network Processor (NP) 316
DMA Interface and CRC logic 318
Network Ports 320

Figure 3

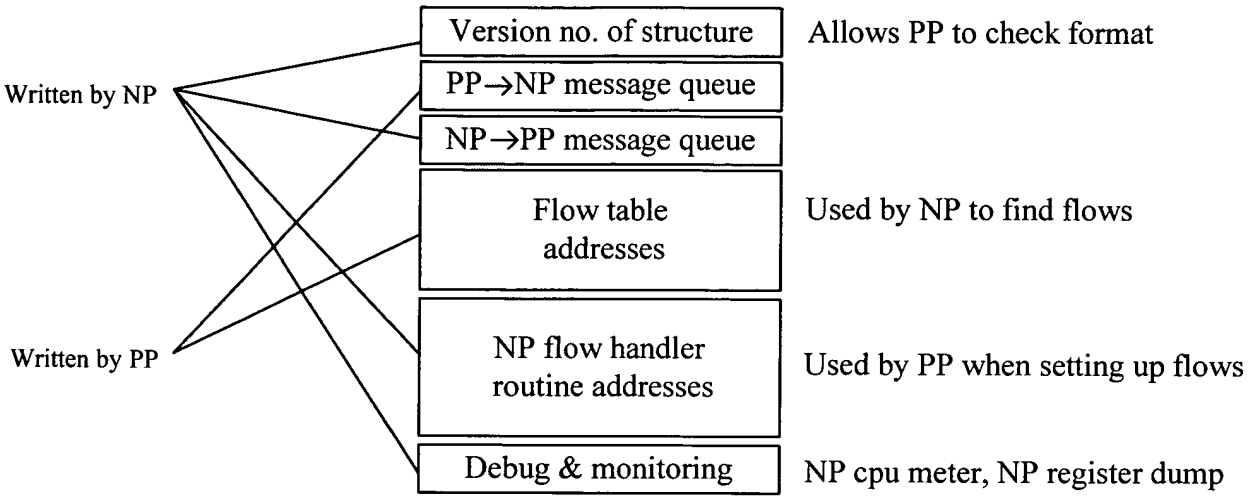
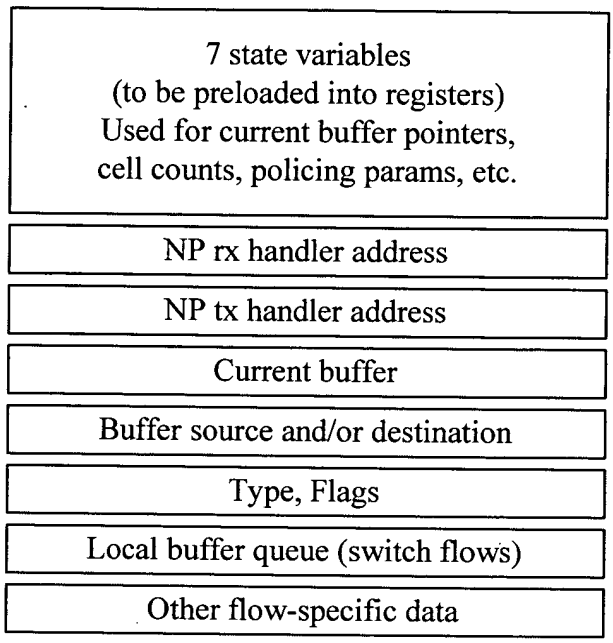

Written by NP
Written by PP
Version no. of structure
PP→NP message queue
NP→PP message queue
Flow table addresses
NP flow handler routine addresses
Debug & monitoring
Allows PP to check format
Used by NP to find flows
Used by PP when setting up flows
NP cpu meter, NP register dump

Figure 4



First part has a similar format in all flows.
A flow is invoked by a single instruction:
- loads 8 or 9 registers
- jumps to handler routine

Figure 5

(These steps are interleaved with operations on other flows and ports)

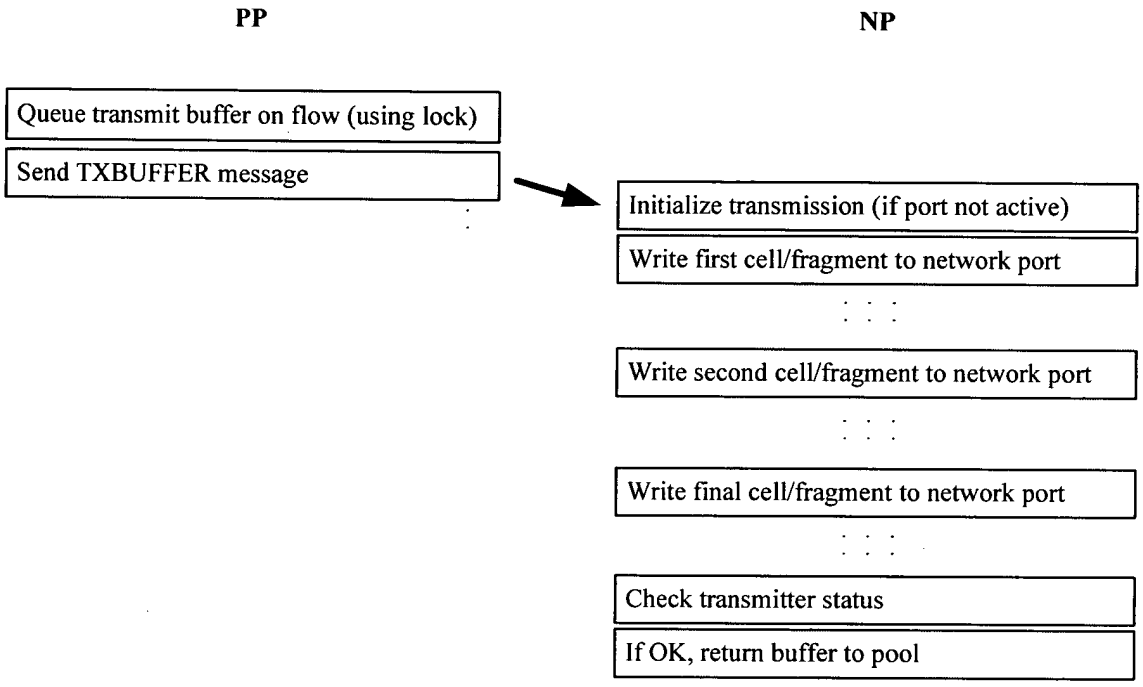


Figure 6

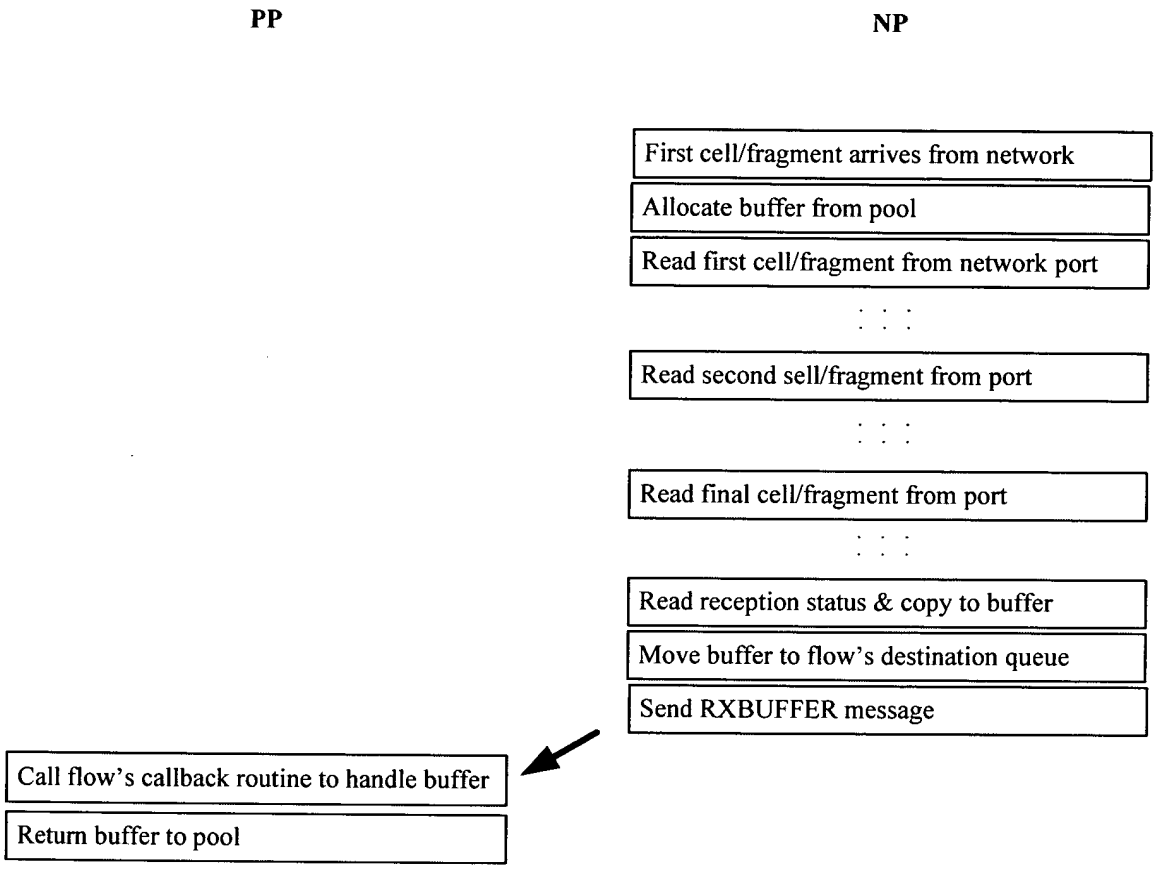

PP
NP
First cell/fragment arrives from network
Allocate buffer from pool
Read first cell/fragment from network port
Read second sell/fragment from port
Read final cell/fragment from port
Read reception status & copy to buffer
Move buffer to flow's destination queue
Send RXBUFFER message
Call flow's callback routine to handle buffer
Return buffer to pool

Figure 7

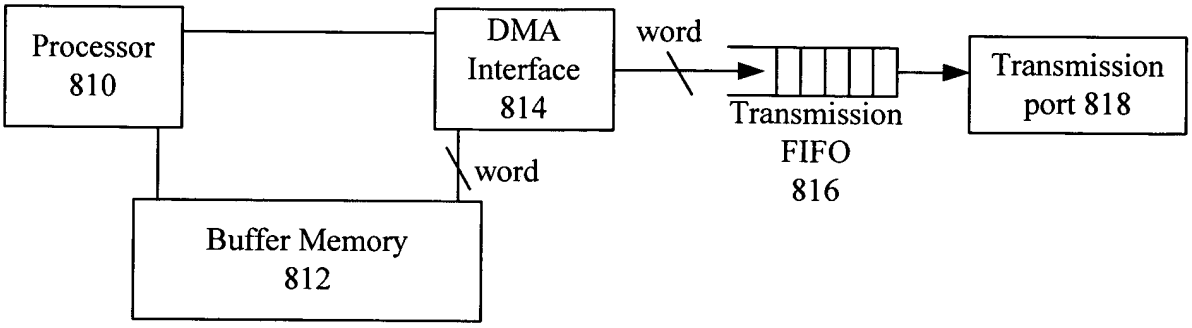

Processor
810
DMA
Interface
814
word
Transmission
FIFO
816
Transmission
port 818
word
Buffer Memory
812

Figure 8

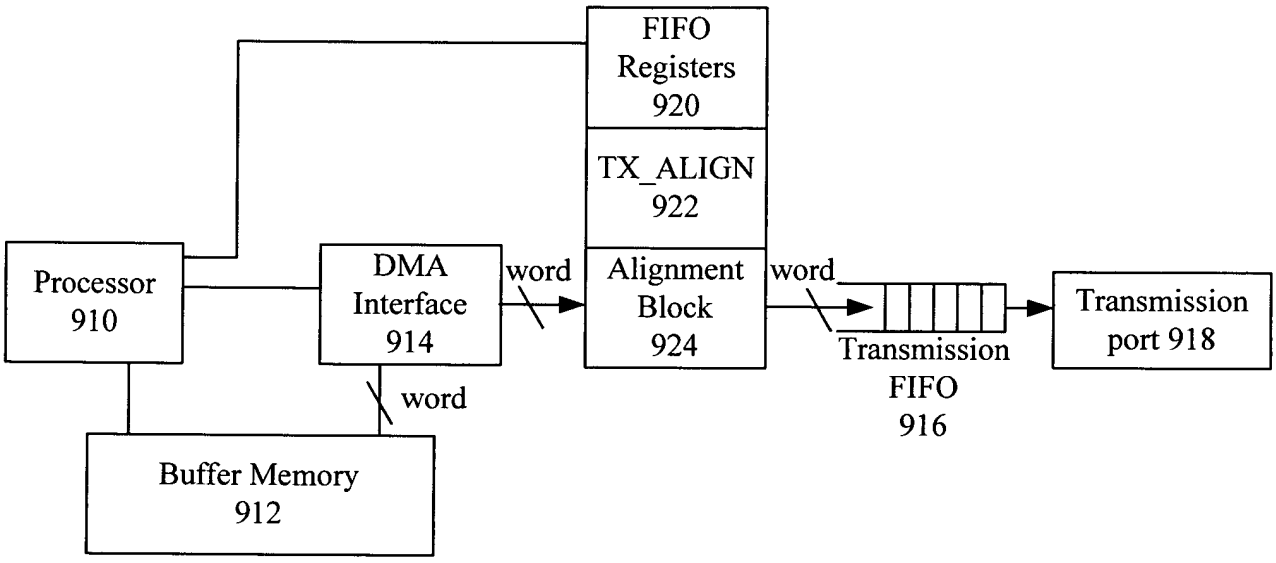

FIFO
Registers
920
TX_ALIGN
922
Processor
910
DMA
Interface
914
word
Alignment
Block
924
word
Transmission
port 918
Transmission
FIFO
916
word
Buffer Memory
912

Figure 9

OCTETS field in TX_ALIGN register	Least significant 2 bits of DMA address	KEEP_ ALIGN flag	TX_ALIGN register word at start	Next word from memory	TX_ALIGN register word after first memory cycle	Word written to FIFO
XX	00	0	XXXX.XXXX	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
XX	01	0	XXXX.XXXX	pqrs.vwXX	pqrs.vw01	No write
XX	10	0	XXXX.XXXX	pqrs.XXXX	pqrs.XX02	No write
XX	11	0	XXXX.XXXX	pqXX.XXXX	pqXX.XX03	No write
00	00	1	XXXX.XX00	pqrs.vwyz	XXXX.XX00	pqrs.vwyz
00	01	1	XXXX.XX00	pqrs.vwXX	pqrs.vw01	No write
00	10	1	XXXX.XX00	pqrs.XXXX	pqrs.XX02	No write
00	11	1	XXXX.XX00	pqXX.XXXX	pqXX.XX03	No write
01	00	1	ghij.kl01	pqrs.vwyz	pqrs.vw01	yzgh.ijkl
01	01	1	ghij.kl01	pqrs.vwXX	pqrs.XX02	vwgh.ijkl
01	10	1	ghij.kl01	pqrs.XXXX	pqXX.XX03	rsgh.ijkl
01	11	1	ghij.kl01	pqXX.XXXX	XXXX.XX00	pqgh.ijkl
10	00	1	ghij.XX02	pqrs.vwyz	pqrs.XX02	vwyz.ghij
10	01	1	ghij.XX02	pqrs.vwXX	pqXX.XX03	rsvw.ghij
10	10	1	ghij.XX02	pqrs.XXXX	XXXX.XX00	pqrs.ghij
10	11	1	ghij.XX02	pqXX.XXXX	pqgh.ij01	No write
11	00	1	ghXX.XX03	pqrs.vwyz	pqXX.XX03	rsvw.yzgh
11	01	1	ghXX.XX03	pqrs.vwXX	XXXX.XX00	pqrs.vwgh
11	10	1	ghXX.XX03	pqrs.XXXX	pqrs.gh01	No write
11	11	1	ghXX.XX03	pqXX.XXXX	pqgh.XX02	No write

Figure 10

OCTETS field in TX_ALIGN register	TX_ALIGN register word at start	Word written to FIFO register	FIFO register written	TX_ALIGN after FIFO register write	Word written to FIFO
00	XXXX.XX00	pqrs.vwyz	TX_FIFO0	XXXX.XX00	pqrs.vwyz
00	XXXX.XX00	XXrs.vwyz	TX_FIFO1	rsvw.yz01	No write
00	XXXX.XX00	XXXX.vwyz	TX_FIFO2	vwyz.XX02	No write
00	XXXX.XX00	XXXX.XXyz	TX_FIFO3	yzXX.XX03	No write
01	ghij.kl01	pqrs.vwyz	TX_FIFO0	pqrs.vw01	yzgh.ijkl
01	ghij.kl01	XXrs.vwyz	TX_FIFO1	rsvw.XX02	yzgh.ijkl
01	ghij.kl01	XXXX.vwyz	TX_FIFO2	vwXX.XX03	yzgh.ijkl
01	ghij.kl01	XXXX.XXyz	TX_FIFO3	XXXX.XX00	yzgh.ijkl
10	ghij.XX02	pqrs.vwyz	TX_FIFO0	pqrs.XX02	vwyz.ghij
10	ghij.XX02	XXrs.vwyz	TX_FIFO1	rsXX.XX03	vwyz.ghij
10	ghij.XX02	XXXX.vwyz	TX_FIFO2	XXXX.XX00	vwyz.ghij
10	ghij.XX02	XXXX.XXyz	TX_FIFO3	pqgh.ij01	No write
11	ghXX.XX03	pqrs.vwyz	TX_FIFO0	pqXX.XX03	rsvw.yzgh
11	ghXX.XX03	XXrs.vwyz	TX_FIFO1	XXXX.XX00	rsvw.yxgh
11	ghXX.XX03	XXXX.vwyz	TX_FIFO2	vwyz.gh01	No write
11	ghXX.XX03	XXXX.XXyz	TX_FIFO3	yzgh.XX02	No write

Figure 11

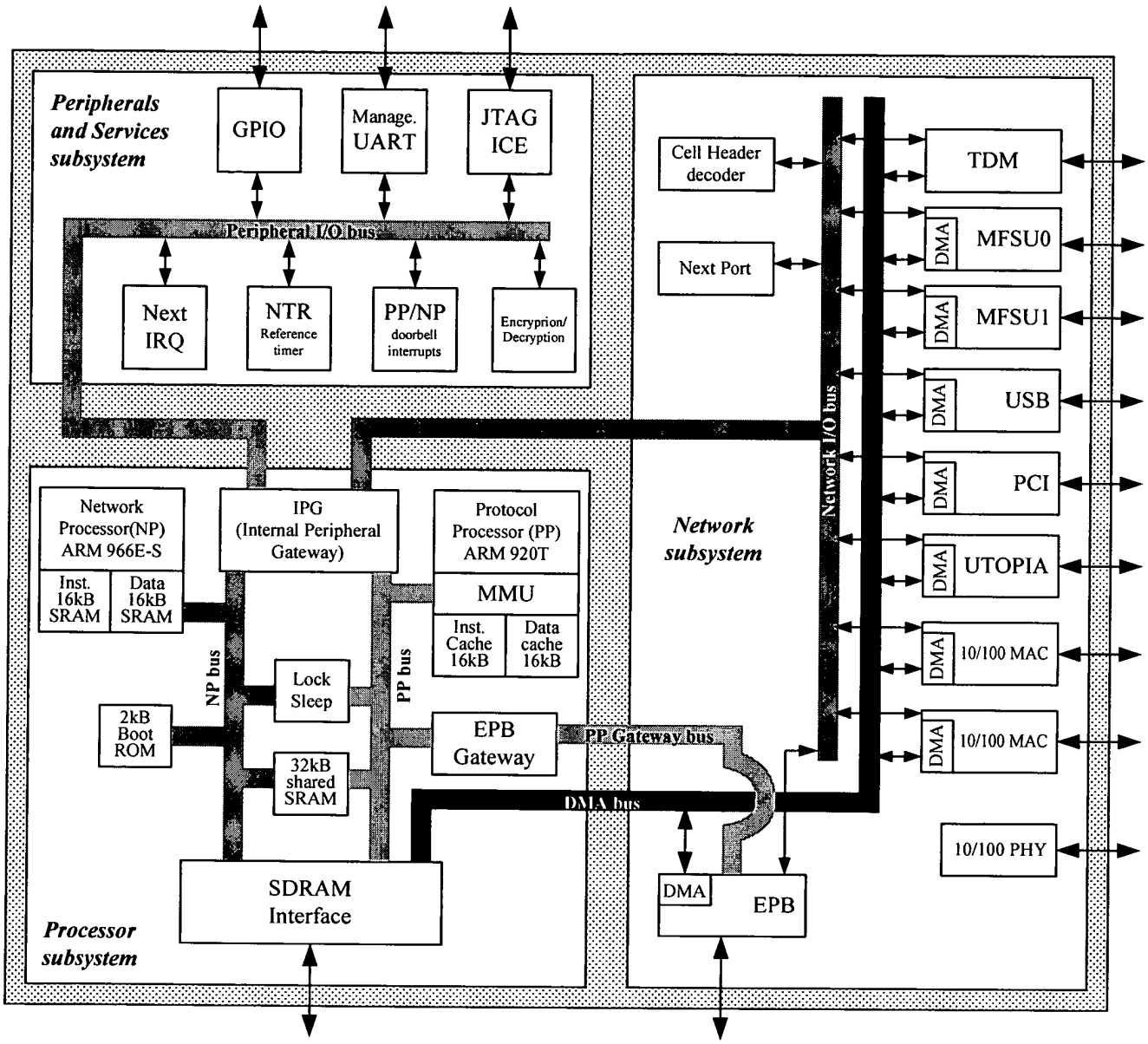

Peripherals and Services subsystem
GPIO
Manage. UART
JTAG ICE
Peripheral I/O bus
Next IRQ
NTR
Reference timer
PP/NP
doorbell interrupts
Encryprion/ Decryption
Network Processor(NP) ARM 966E-S
Inst. 16kB SRAM
Data 16kB SRAM
IPG (Internal Peripheral Gateway)
Protocol Processor (PP) ARM 920T
MMU
Inst. Cache 16kB
Data cache 16kB
NP bus
PP bus
Lock Sleep
2kB Boot ROM
32kB shared SRAM
EPB Gateway
PP Gateway bus
DMA bus
SDRAM Interface
Processor subsystem
Network subsystem
Network I/O bus
Cell Header decoder
Next Port
DMA
EPB
TDM
MFSU0
MFSU1
USB
PCI
UTOPIA
10/100 MAC
10/100 MAC
10/100 PHY

Figure 12

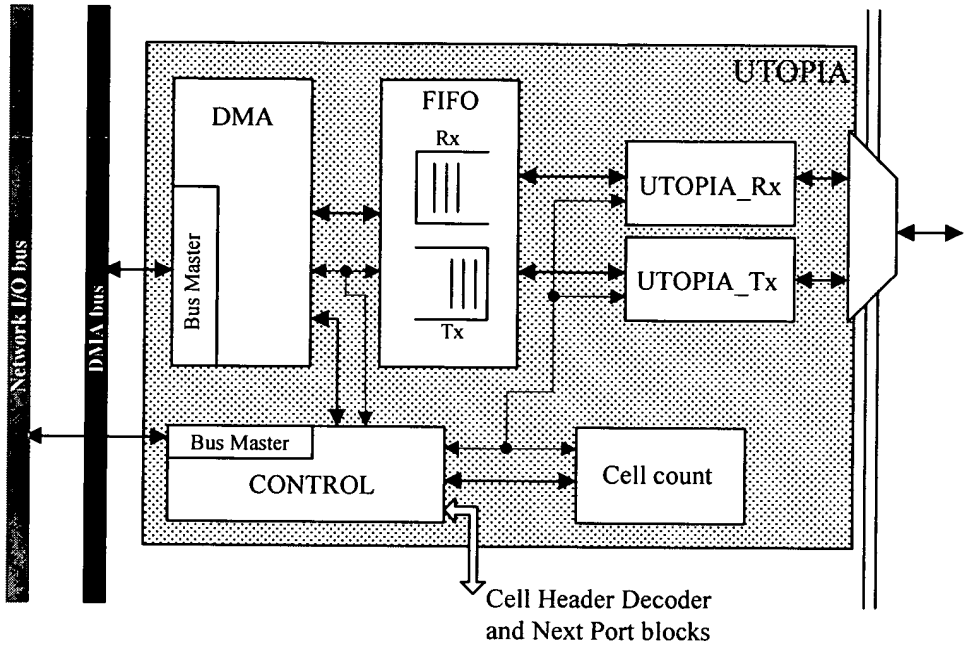

Network I/O bus
DMA bus
UTOPIA
DMA
Bus Master
FIFO
Rx
Tx
UTOPIA_Rx
UTOPIA_Tx
Bus Master
CONTROL
Cell count
Cell Header Decoder
and Next Port blocks

Figure 13

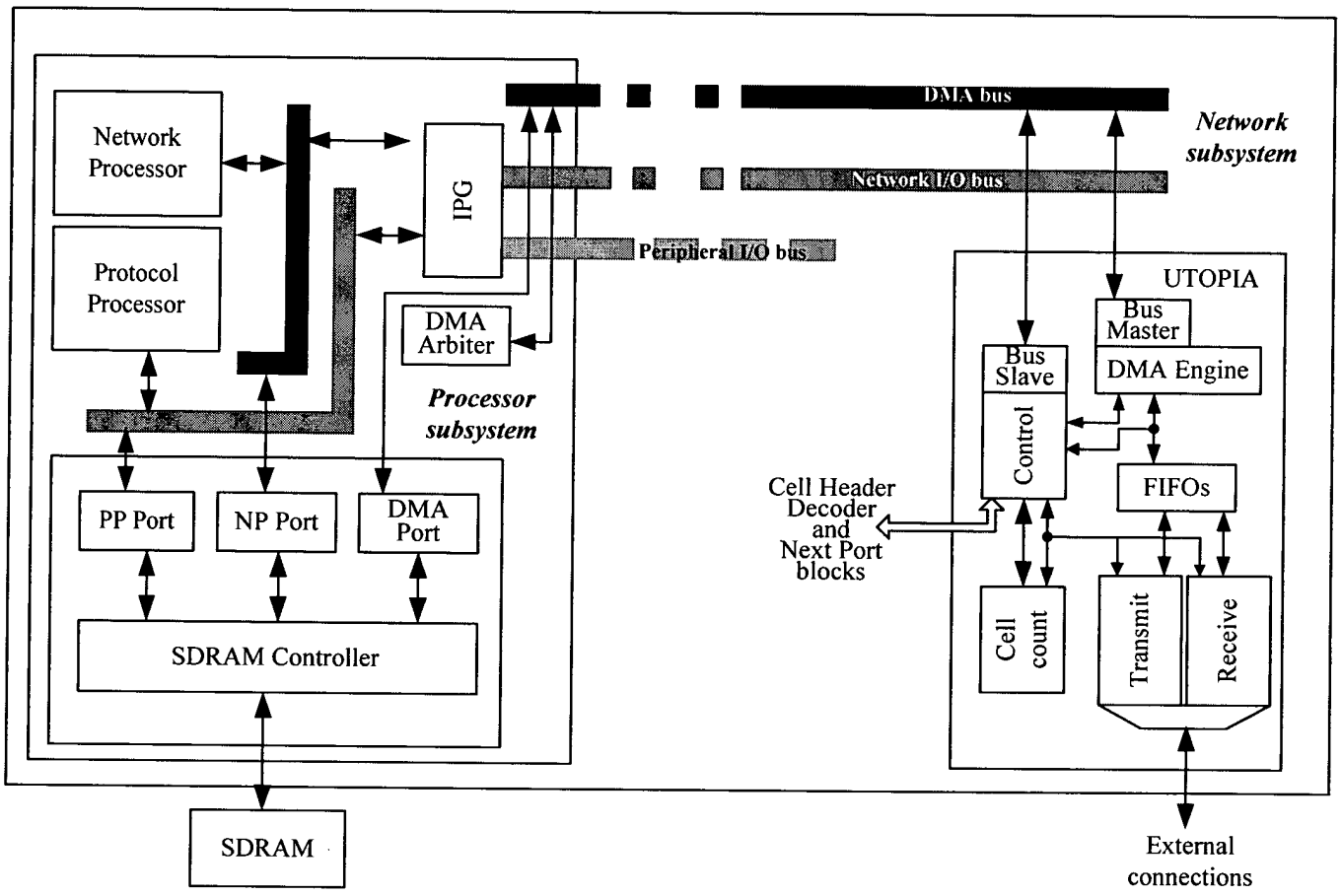

Network Processor
Protocol Processor
IPG
DMA Arbiter
Processor subsystem
PP Port
NP Port
DMA Port
SDRAM Controller
SDRAM
DMA bus
Network I/O bus
Peripheral I/O bus
Network subsystem
UTOPIA
Bus Master
Bus Slave
DMA Engine
Control
FIFOs
Cell Header Decoder and Next Port blocks
Cell count
Transmit
Receive
External connections

Figure 14

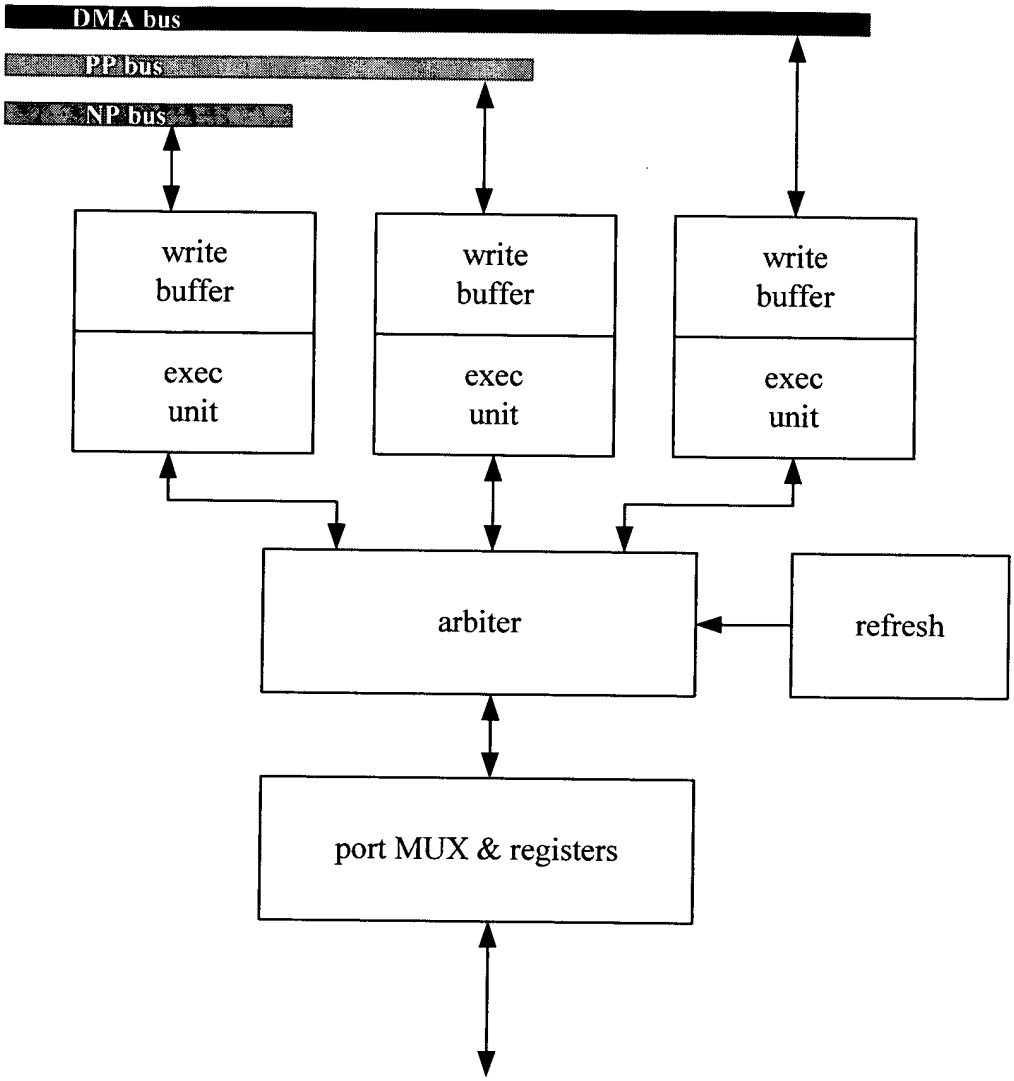

DMA bus
PP bus
NP bus
write buffer
exec unit
write buffer
exec unit
write buffer
exec unit
arbiter
refresh
port MUX & registers

Figure 15

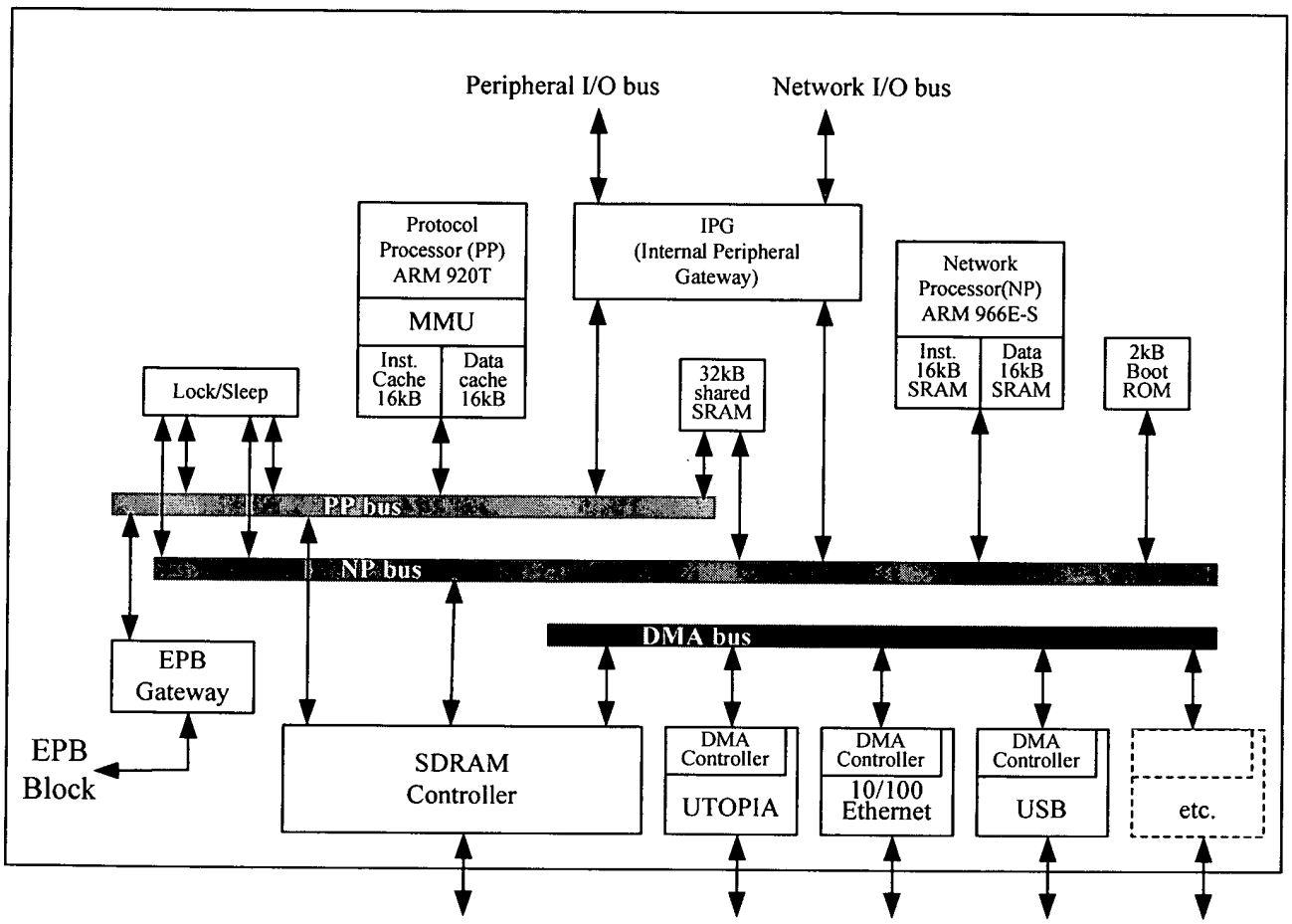

Peripheral I/O bus
Network I/O bus
Protocol Processor (PP) ARM 920T
MMU
Inst. Cache 16kB
Data cache 16kB
IPG (Internal Peripheral Gateway)
Network Processor(NP) ARM 966E-S
Inst. 16kB SRAM
Data 16kB SRAM
2kB Boot ROM
32kB shared SRAM
Lock/Sleep
PP bus
NP bus
DMA bus
EPB Gateway
EPB Block
SDRAM Controller
DMA Controller
UTOPIA
DMA Controller
10/100 Ethernet
DMA Controller
USB
etc.

Figure 16

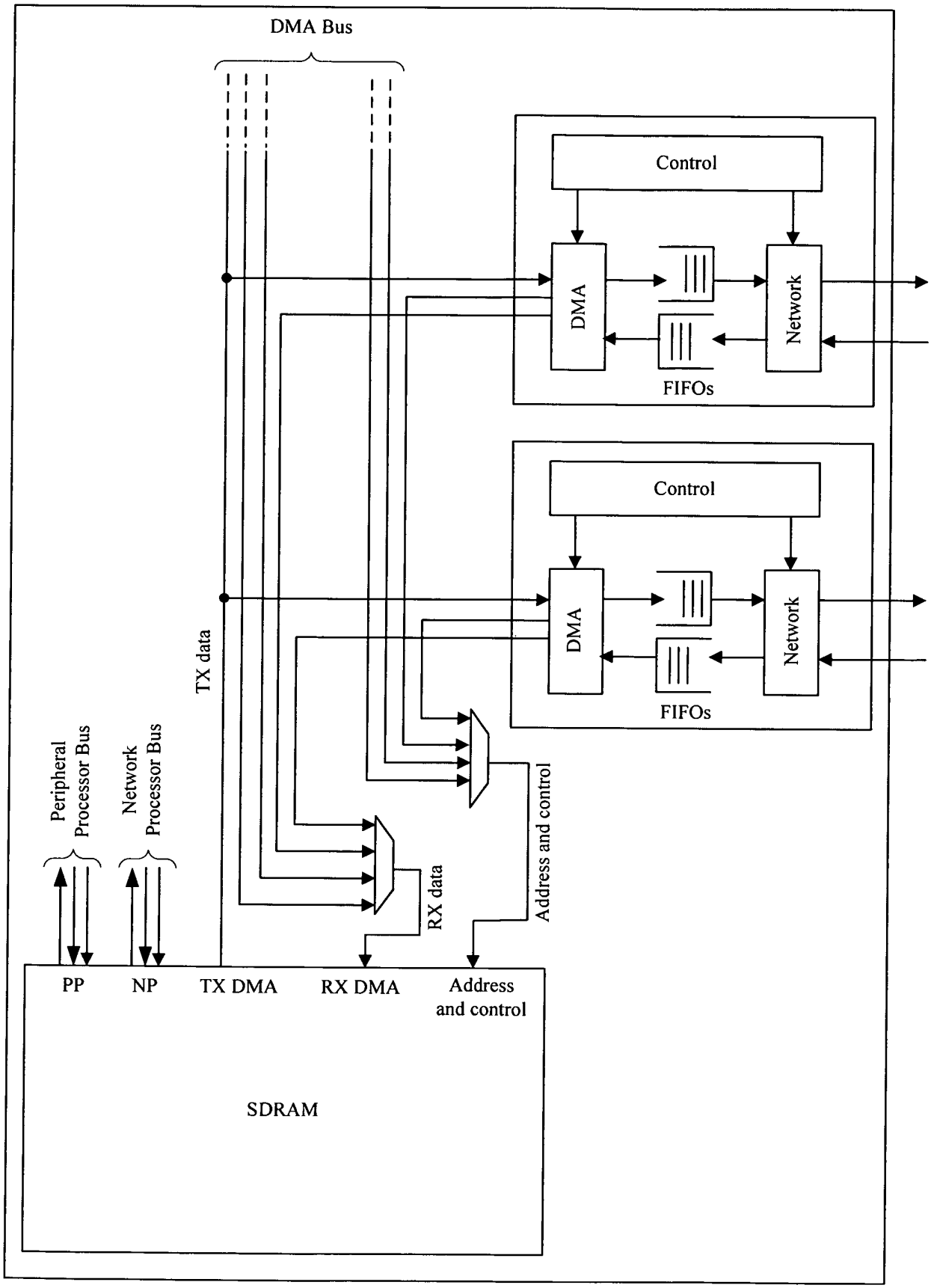

DMA Bus
Control
DMA
Network
FIFOs
Control
DMA
Network
FIFOs
TX data
Peripheral Processor Bus
Network Processor Bus
RX data
Address and control
PP
NP
TX DMA
RX DMA
Address and control
SDRAM

Figure 17